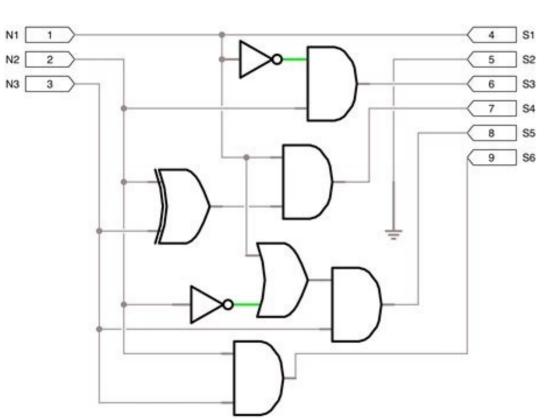
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## Logic gates statement questions. Logic gates short questions and answers.

And if 0 is applied to anode and 1 to cathode Diode acts as open circuit i.e. OFF. The logic gates which are derived grown to a long side the traditional symbols for the India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question: \(Y = {\bf{A}}\) \oplus {\bf{B}} = \bar AB + A\bar B\) Key Points: 1) The output is low or '0' when both the inputs are the same. OR Gate NAND Gate Ans. OR gate AND gate NOT gate None of the above Ans. 3 Q14. The logic gate that will have HIGH or "1" at its output when any one of its inputs is HIGH is a/an ................ gate. Note: 74 LS 32  $\rightarrow$  Quad 2-Input EXOR Gate 74 HC 08  $\rightarrow$  Quad 2-Input EXOR Gate 7 ..... NAND and NOR gates are universal gates. The figure below India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students Answer (Detailed Solution Below) 8 B = X0. shows the IEEE/ANSI symbols alongside the traditional symbols for the basic gates: Calculation: Given Boolean expression is, F = AB + AC + BC = ABC + ABCPractice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167 + Students Concept: Name of Law A • A = A A + A = A Idempotent Law A • A = A A + A = A Idempotent Law A • A = B + A Distributive Law  $(A \bullet B) C = A (B \bullet C) (A + B) + C = A + (B + C)$  Absorption Law  $A (A + B) = A + A + A \bullet B = A$  De Morgan Law  $(A \bullet B)' = A' + B' (C + C') F = AB + AB' (C + C') F = AB +$ Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students NAND and NOR gates AND, OR, NOT gates are the basic gates. 1 Q6. Digital .... OR gates NOT gates NAND gates None of the above Ans. 5) 4 NAND & 5 NOR logic gates required for realization of XOR gate . 4 Q18. A NAND gate has ....... T = 2n Tpd Here 2 is multiplied with the propagation delay when logic gates are connected in feedback. 3 XOR GATE Symbol: Truth Table: Input A Input B Output Y = A \underset B 0 0 0 0 1 1 1 0 Output Equation: \(Y = {\bf{A}} \operator B + A \bar B\) Key Points: 1) If B is always High, the output is low when both the inputs are different. Case 3 When A is logic 1 and B is logic 0 Then the logic of C will be 1. 1 Q9. In Boolean algebra, the bar sign (-) indicates .......... ..... 3 Q10. An OR gate has 4 inputs. A B C = A . (Y=A.) overline {B}+ overline {A}.B) A B Y 0 0 0 0 1 1 1 0 1 1 1 0 India's #1 Learning Platform Start Complete Exam Preparation Daily Live Master Classes Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167 + Students ( $\bar{A} + \bar{B}$ ) ( $\bar{C} + \bar{D}$ ) ( $\bar{E} + \bar{F}$ ) AB + CD + EF(A + B) ( $\bar{C} + \bar{D}$ ) ( $\bar{C} +$ \;\overline {C.D\;} + \;\overline {EF\;} }\) Z = AB + CD + EF India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students EX-NOR Gate: Symbol: Truth Table: Input A Input B Output Y = A B 0 0 1 0 1 0 1 1 0 0 1 1 1 From the truth table, the output is one when both A and B are equal logic. inputs and ...... Low High alternately high and low may be high or low depending on relative magnitude of inputs Ans. 7400: 74HC00 is a 14-Pin Quad 2-Input NAND Gate IC (Integrated Circuit). India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students XNOR Gate: Symbol: Truth Table: Input A Input B Output \(Y={\overline} A\oplus B}\) New Points: 1) If B is always Low, the output is the inverted value of the other input A, i.e. A. India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students C = ABC = A + B\(C = \overline \{A + B\}\)\(C = \overline \{A + B\}\)\(C = \overline \{A + B\}\) Logic 1 means High and Logic 0 means low. Explanation: The given logic circuit is For different logic of A and B,4 cases are there and according to that logic of C will vary. (X1  $\oplus$  X2) \((A = \overline {X 0}}\) Case 1 When X0 = 1 A = 0 and C = 0 output Y = C + X3 = X3 Thus in both cases. Logic Gates Min. 7486: 74HC86 is a Quad 2-Input EXOR Gate 14 Pin IC. OR gate AND gate INVERTER gate Comparator Ans. 2 Q11. Both OR and AND gates can have only two inputs. The Boolean equation of output can be written as: Output = AB + AB Output Equation: Y = AOB Key Points: 1) If B is always Low, the output is the inverted value of the other input A, i.e.  $\bar{A}$ . A B C = A + B 0 0 0 0 1 1 1 0 1 1 1 1 NOT Gate: The Logic NOT Gate is the most basic of all the logic gates and is often referred to as an Inverting Buffer or simply an Inverter. Hence XOR gate can be used to know whether two digital inputs are identical. B 0 0 0 0 1 1 1 0 1 1 1 1 NOT Gate: The Logic OR Gate is a digital logic circuit whose output goes HIGH only when any one or more than one of its inputs is HIGH. The general representation of all the minterms using 3-variables is shown below. 3 Q20. Ans. 3 When all three diodes are reversed biased (open-circuited), then the output will get grounded and the circuit will give 0 as output. truth table entries are necessary for a four-input circuit. 1) The output is low when both the inputs are the same. 2) The output is high noise immunity and the ability to drive 10 LS-TTL loads. Internal circuit is composed of three stages, including a buffer output which provides high noise immunity ...... NOT gate OR gate AND gate None of the above Ans. XOR and XNOR are the derived gates. inverted value of the other input B, i.e. \$\overline{B}\$ 2) The output is low only when both the inputs are high 3) It is a universal gate India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students XOR GATE Symbol: Truth Table: Input A Input B Output Y = A \undark B 0 0 0 0 1 1 1 0 1 1 1 0 Output Equation: \(Y = {\\bf{A}}\) \(Y = \\bf{A}\) Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167 + Students The number of 2-input NAND gates required to implement a 2-input XOR gate is 4. 2) The output is low when both the inputs are different. Whenever in diode, if 1 is applied to anode and 0 to cathode then Diode acts as a short circuit i.e. ON. number of NAND Gate NOT 1 1 AND 3 2 OR 2 3 EX-OR 5 4 EXNOR 4 5 NAND 4 1 NOR 1 4 Half-Adder 5 5 Half-Subtractor 5 5 Full-Adder 5 Started for Free Download App Trusted by 2,71,73,167+ Students \(Q = \overline \{AB} \) Output expression Q is equivalent to NAND gates and NOT gates Ans. 4) It is mostly used in parity generation & detection. 1 Q3. The inputs of a NAND gate are connected together. If inputs are the same, the output will be LOW '0'. 1 Q15. Symbol: Truth Table: Input A Input B Output \(Y={\overline}A\) NAND Gate: The logic Gate Name AND Form OR Form Identity law 1.A=A 0+A=A Null Law 0.A=0 1+A=1 Idempotent Law A.A=A A+A=A Inverse Law AB=B+A Associative Law (AB)C (A+B)+C = A+(B+C) Distributive Law A+BC=(A+B)(A+C) A(B+C)=AB+AC Absorption Law A(A+B)=A A+AB=A De Morgan's Law (AB)'=A'+B' (A+B)'=A'B' BC +  $A\overline{C}AB$  Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students Y=0, Z=0Y=1, Z=0Y=1, Z=0Y=1, Z=0Y=1, Z=1 After the simplification, we can redraw the given logic circuit as So that, Y=XX and Y=XX and Y=XX are Y=XX and Y=XX and Y=XX are Y=X and Y=X are Y=X are Y=X and Y=XPlatform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students The given gate is an XNOR gate. NOR gate is an XNOR gate is an XNOR gate is an XNOR gate. a logic level 1 only when both of its inputs are different. One input is high and the other three are low. Logic level gates Tpd is the propagation delay of one gate Calculation: Given, n = 3 as there are three gates with feedback Tpd = 100 nsec  $T = 2 \times 3 \times 10^{-7}$  T=  $6 \times 10^{-7}$  Fundamental Frequency is given by  $f (f = \frac{1}{6} \times 10^{-7})$  f = 1.67 × 106 f = 1.67 MHz India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students A 2 input logic gate which has always a high output when its inputs are different. .......... output Y = X3 output Y will be 1, when X3 = 1 Favourable cases: x3 x2 x1 x0 1 0 AND Gate is a digital logic circuit whose output HIGH only when all the inputs are 1 (HIGH) otherwise the output will be LOW. Stop signal Invert input signal Act as a universal gate None of the above Ans. 3) The output is high when both the inputs are the same. 2) The output is high when both the inputs are the same. At least one input is HIGH At least one input is LOW All inputs are HIGH All inputs are LOW Ans. This device contains four independent gates each of which performs the logic NAND function. number of NAND Gate NOT 1 1 AND 3 2 OR 2 3 EX-OR 5 4 EXNOR 4 5 NAND 4 1 NOR 1 4 Half-Adder 9 9 Full-Subtractor 9 9 India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students The figure below shows the IEEE/ANSI symbols alongside the traditional symbols for the basic gates: Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students 7432: 74LS32 is a Dual input OR Gate with Quad package. It contains four independent gates each of which performs the logic or function. 3 Q19. The basic logic gate whose output is the we make a table A B C 0 0 0 0 1 1 1 0 1 1 1 This Table is of Logic OR gate. 2 Q8. When an input signal 1 is applied to a NOT gate produces an output only when the two inputs are same. NAND circuits are contained in a 7400 NAND IC. It is advanced high speed CMOS with the low power consumption of standard CMOS integrated circuits. 7408: 74HC08 is a Quad 2-Input AND Gate 14 Pin IC. 2) The output is high when both the inputs are different. The implementation of other gates using only NOR gate is as shown: Logic Gates Min. 1 Q2. The inverter is ................................. NOT gate OR gate AND gate None of the above Ans. India's #1 Learning Platform Start Complete Exam Preparation Daily Live MasterClasses Practice Question Bank Mock Tests & Quizzes Get Started for Free Download App Trusted by 2,71,73,167+ Students 1 GHz0.5 GHz3.34 MHz1.67 MHz Concept: Propagation Delay: The propagation Delay, or gate delay, is the length of time that starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. Case 1 When A is logic 0 and B is logic 0 and B is logic 0 and B is logic of C will be 0. \(Y=\overline {A.B}\) A B Y 0 0 1 0 1 1 1 0 NOR Gate: The logic Gate is obtained after adding NOT Gate after OR Gate. XNOR Gate: Symbol: Truth Table: Input A Input B Output \(Y={\overline{A\oplus B}}\) 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 Output Equation: \(Y={\overline{A\oplus B}}\) Key Points: 1) If B is always Low, the output is the inverted value of the other input A, i.e. \(\bar{A\oplus B}}\)

11/03/2022 · Solve each of the following equations. Express your final answers as algebraic expressions where possible: (1) z^3+27i=0 (2) z^2=3-4i; Show work and dot down answers on paper only please, it helps with understanding and making things easier to follow and it's more clear. Thank you school. The stops he used to conduct the survey are l... Risk-Based Inspection (RBI) is an analysis methodology and process that, as opposed to condition-based inspection, requires qualitative or quantitative assessment of the probability of failure (PoF) and the consequence of failure (CoF) associated with each equipment item, piping circuits included, in a particular process unit. A properly-implemented RBI program categorizes ... This is the logic diagram of a single bit full adder made from digital logic gates. Each input lines provide the sum and carry out in form of bits. Related Post: Different Types of Sensors with Applications. Riser Diagram

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